**University of Asia Pacific**

**Department of Computer Science and Engineering**

**Mid-Semester Examination Fall-2020**

**Program: B.Sc. in CSE**

Course Title: Design and Testing of VLSI Course No. 457 Credit: 3.00 Time: 1.00 Hour. Full Mark: 60 There are Four Questions. Answer three questions including Q-1 and Q-2.

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| 1. | a. | Discuss the impact of Moore’s law in the IC fabrication industry. Include relevant graph and explanation where applicable. | **10** |
|  | b. | Draw the schematic diagram of AND-AND-OR-INVERT or A2O2I. | **10** |
| 2. |  | Consider a wafer with Defect density 2.5 defects/cm2, clustering parameter 0.5, chip width 6mm, chip length 7mm. Each wafer has 100 chips. The cost of processing a wafer is BDT (YOUR FULL REGISTRATION NUMBER).   * Calculate the processing cost per chip. * Calculate the processing cost per chip if Design for testability (DFT) is included, which increases the chip area by 10% | **20** |
| 3. | a. | Explain non ideal I-V of MOS with a graph. | **10** |
|  | b. | Prove that n-input NAND gate has a certain logical effort. | **10** |
|  |  | **OR** |  |
| 4. | a. | Explain C-V characteristics of MOS with a graph. | **10** |
|  | b. | Prove that n-input NOR gate has a certain logical effort. | **10** |